Dynamics Of A PLL Timebase

Analyzing A Phase Locked Loop Synthesized Timebase

The clock generator in a digital oscilloscope is a prime example of the use of a phase locked loop (PLL) frequency synthesizer. LeCroy scopes use a PLL to frequency multiply a precision 10 MHz reference oscillator to either 400 or 500 MHz. These sampling clocks can then be counted down to create lower sampling frequencies. The block diagram of a typical PLL frequency multiplier is shown in figure 1.

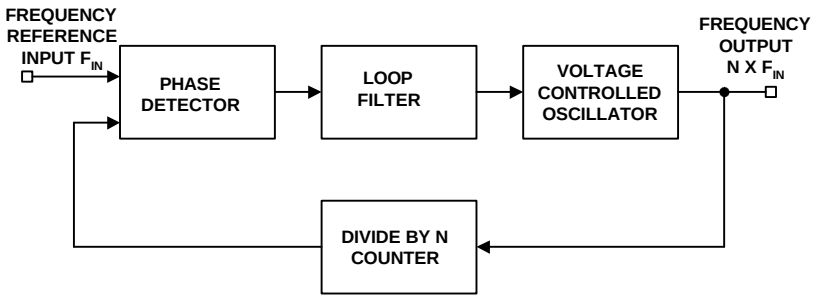

Figure 1 – Block diagram of a PLL frequency multiplier

In addition to basic functional tests designers may measure the dynamic response of the PLL to changes in the reference frequency. This is important in LeCroy oscilloscopes because we allow users, with option CKTRIG, to use their own 10 MHz frequency reference as a reference source for the scope's timebase.

Figure 2 shows the input to the external reference input used to measure the step response of the PLL. The reference frequency is a nominal 10 MHz sine with a 100 kHz step (9.95 – 10.05 MHz) as shown in the top trace of figure 2. The jittertrack function of frequency, trace B, is used to show the instantaneous frequency of the reference input. This signal is averaged to remove random variations that are not synchronous with the step change, as shown in trace C. Note that the frequency deviation of 100 kHz is read using cursors on the averaged trace. The step change in the input is very clean with no obvious overshoot or ringing. Trace A, Jittertrack of interval error, shows the instantaneous phase change of the clock relative to a 10 MHz ideal reference. The phase is the integral of the instantaneous frequency (a square wave) and exhibits a triangular waveshape.

The measurement of the output frequency, multiplied by a

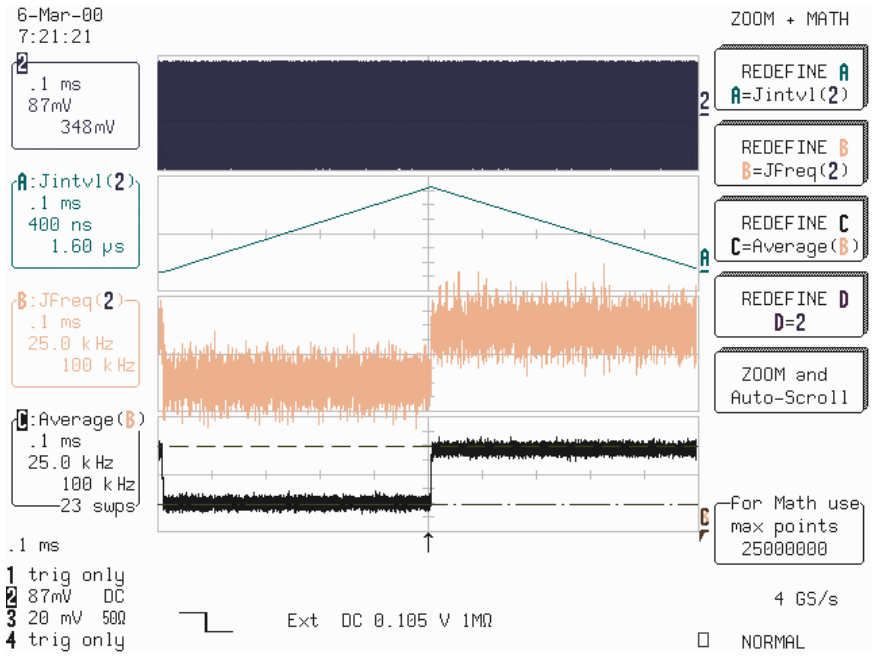

Figure 2 Analysis of the step change in the reference frequency

factor of 3.2, is shown in figure 3. The response of the PLL is delayed as shown by the shift to the right of both the frequency (trace C) and phase (interval error) waveform (trace A). In addition the output frequency overshoots by about 25 % and then recovers within 0.15 ms. There are several glitches on the step edge indicating "hunting" as the control system attempts to track the input change. The lower trace is the control voltage being applied to the voltage controlled oscillator (VCO) in the PLL. It is obvious by the similarity of the PLL output frequency and the control voltage waveforms that the VCO is tracking the control voltage very precisely. This is a good measure of the VCO linearity.

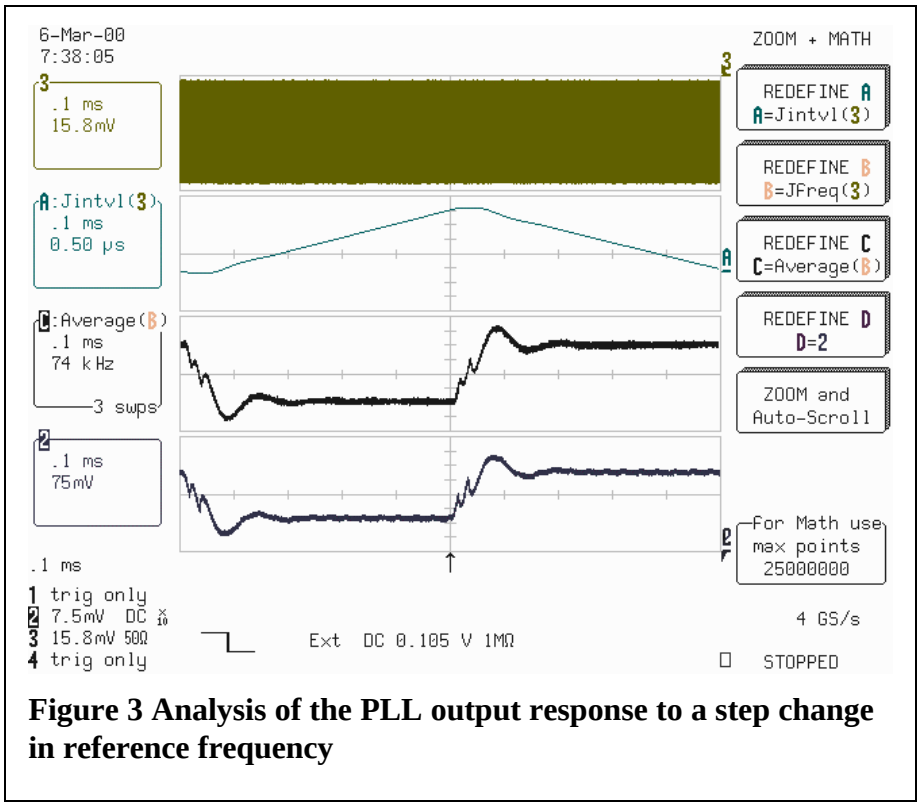

Figure 3 Analysis of the PLL output response to a step change in reference frequency

In figure 4 JitterTrack Frequency function is used to measure the slew rate of the PLL response to a range change in the oscilloscope's time/division setting. The PLL is originally operating with an output frequency of 400 MHz. After the change the timebase is recalibrated at 200 MHz. This is done by changing the countdown path to add a 2:1 stage. It is then returned to 400 MHz and slews, at a rate limited by the VCO, to 500 MHz. Using this measurement it can be determined how long it takes to re-establish specified frequency accuracy after a range change.

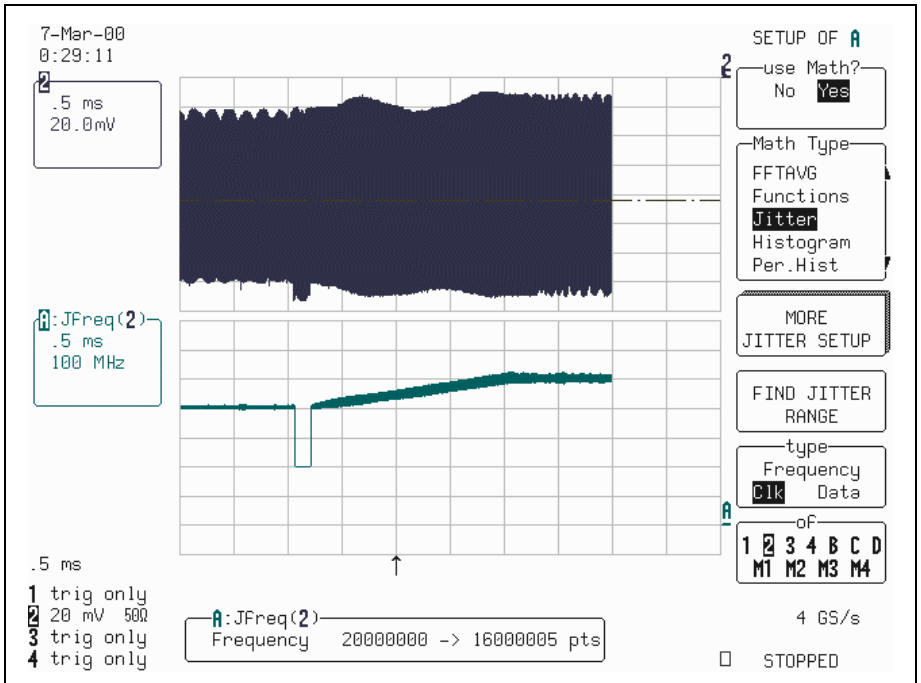

Figure 4 Response of PLL to range change in time/division setting requiring change from 400 to 500 MHz